REMARKS

The Applicant sincerely appreciates the Examiner's thorough examination of the present application as evidenced by the Final Office Action of March 6, 2007 ("the Office Action"). In particular, the Applicant appreciates the Examiner's indication that Claims 9-14, 22-28, 42-51, 55-60, 62, and 63 are allowed. The Applicant further submits that the subject matter of Claims 72-74 is in condition for allowance because no rejections to have been applied to these claims or to any claims from which they depend.

In the following remarks, the Applicant will show that the claims meet all requirements of 35 USC section 112, and that claims 1 and 6 are patentable over Morishita. Accordingly, the Applicant respectfully submits that all claims are in condition for allowance, and a Notice of Allowance is respectfully requested in due course.

Removal Of Finality Is Respectfully Requested

The Applicant respectfully submits that all claims are patentable for at least the reasons set forth below. In the event that any rejections should be maintained, however, the Applicant respectfully requests that the finality of the Office Action be withdrawn because the Office Action was not properly made final. In particular, the Office Action states that:

> Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**

Office Action, page 4. No claim amendments, however, were presented in the most recent Response filed on February 8, 2007 (responsive to the Office Action mailed December 11, 2006). Because there were no amendments to necessitate the new grounds of rejection, the Office Action of March 6, 2007, was improperly made final, and removal of finality of the Office Action is thus respectfully requested. Moreover, no new issues are raised in the present response, because no claim amendments are being presented.

As discussed in greater detail below, all claims of the present application are in condition for allowance. In the event that the Examiner should maintain any existing rejections and/or apply any new rejections, the Applicant respectfully requests issuance of a new non-final Office Action resetting the period for response to allow for appropriate response and consideration thereof.

Withdrawal of All Rejections Under 35 U.S.C. Sec. 112 Is Requested

Claims 1, 9, and 19 have been rejected under 35 U.S.C. Sec. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards at the invention. The Applicant respectfully submits that all claims meet all requirements of 35 U.S.C. Sec. 112 for at least the reasons discussed below.

Regarding Claim 1, the Office Action states that:

> Claim 1 recites the limitation "... the first electrical and mechanical connection bypasses the second integrated circuit substrate... ." However, the instant invention does not disclose the aspect. Rather, Fig. 5 of the instant invention shows that the signal is coupled to the third integrated circuit substrate through the second integrated circuit substrate.

Office Action, page 2.

The Applicant respectfully submits that support for the recitations of Claim 1 are provided, for example, by the illustrated embodiments of Figure 5 as follows. The first integrated circuit substrate of Claim 1, for example, is supported by the substrate 10a of Figure 5; the second integrated circuit substrate of Claim 1, for example, is supported by the substrate 10b of Figure 5; and the third integrated circuit substrate of Claim 1, for example, is supported by the substrate 10c of Figure 5. In addition, the first electrical and mechanical connection of Claim 1, for example, is supported by the large bump 50c of Figure 5 which provides electrical and mechanical connection between the substrates 10a and 10c. While the electrical and mechanical connection provided by the large bump 50c is part of a signal path that traverses the substrate 10b in the illustrated embodiment of Figure 5, the electrical and mechanical connection provided by the large bump 50c bypasses the substrate 10b as shown in Figure 5. Accordingly, the Applicant respectfully submits that Claim 1 meets all requirements of 35 U.S.C. Sec. 112.

As noted above, the Office Action indicates that Claim 9 is rejected under 35 U.S.C. Sec. 112. The Applicant notes, however, that page 4 of the Office Action states that Claim 9 is allowed. Accordingly, it is unclear whether the rejection of Claim 9 under 35 U.S.C. Sec. 112 was intended. Out of an abundance of caution, however, the Applicant will show that Claim 9 meets all requirements of 35 U.S.C. Sec. 112. Regarding Claim 9, the Office Action states that:

> Claim 9 recites the limitation "... device side ... face a first direction and the backsides face a second direction." Note that the instant invention discloses that both the device side and the backside face the PCB. Claims 15, 21 and 29 recite the similar limitation.

Office Action, page 2.

As discussed with respect to Figures 1 and 2a-2b, a device side of a substrate and a backside of the substrate are on opposite sides of the substrate. *See*, Application, page 11, lines 7 – 14, and page 12, lines 10 – 17. Accordingly, the device side of the substrate and the backside of the substrate face opposite directions, and the device side of the substrate and the backside of a same substrate cannot both face the printed circuit board as suggested by the Office Action. Moreover, Figure 5 shows that device sides of the substrates 10a, 10b, and 10c face the substrate 210 (such as a printed circuit board PCB), while backsides of the substrates 10a, 10b, and 10c face away from the substrate 210. Accordingly, the Applicant respectfully submits that Claim 9 meets all requirements of 35 U.S.C. Sec. 112. The Applicant further submits that Claims 15, 21, and 29 also meet all requirements of 35 U.S.C. Sec.112.

Regarding claim 19, the Office Action states that the recitation "a direct electrical coupling is provided between the signal path and an electronic circuit of the fifth integrated circuit substrate, and wherein the signal path is free of a direct electrical coupling with an any electronic circuit of the third integrated circuit substrate" is not disclosed. *See*, Office Action, page 2. In support of the rejection of claim 19, the Office Action states that:

> Rather, Fig. 5 of the instant invention shows that the signal is coupled to the third integrated circuit substrate through the fourth integrated circuit substrate.

Office Action, page 2. The Office Action further states that Claims 52 and 75 recite the similar limitation.

The Applicant respectfully notes that a unique signal path for a memory device is discussed, for example, with respect to Figure 6 at page 16, line 3 to page 18, line 21 of the Application as originally filed. A portion of a signal path may thus be provided on an integrated circuit substrate without providing a direct electrical coupling with any electronic circuit of the integrated circuit substrate. Accordingly, all recitations of Claim 19 are supported in the Application as originally filed. In addition, all recitations of Claims 52 and 75 are also supported for reasons similar to those discussed above with respect to Claim 19.

The Applicant thus submits that all recitations of Claims 1, 9, 15, 19, 21, 29, 52, and 75 are fully supported in the Application as originally filed for at least the reasons discussed above. In addition, the recitations that the Examiner has objected to are included in the Claims as originally filed. For example, recitations relating to a first electrical and mechanical connection bypassing a second substrate were included in Claim 1 as originally filed; recitations relating to device sides facing one direction and backsides facing another direction were included in Claims 9 and 15 as originally filed; and recitations relating to a signal path being free of a direct electrical coupling with any electronic circuit of an integrated circuit substrate were included in Claim 19 as originally filed.

Accordingly, the Applicant respectfully requests that all rejections under 35 USC Section 112 be withdrawn. The Applicant further submits that Claims 9-19, 21, 29-31, 33-40, 52, 66-67, 69-71, and 75-79 are in condition for allowance because all rejections under 35 USC Section 112 have been overcome, and no art rejections have been applied to these claims. In the following remarks, the Applicant will also show that Claims 1 and 6 are patentable over the cited art.

Claims 1 And 5 Are Patentable Over The Cited Art

Claims 1 and 6 have been rejected under 35 USC Section 102(e) as being anticipated by U.S. Patent No. 6,392,292 to Morishita (Morishita). The Applicant respectfully submits, however, that Claims 1 and 6 are patentable over Morishita for at least the reasons discussed below. More particularly, independent Claim 1 recites, an electronic device comprising:

> a first integrated circuit substrate;
> a second integrated circuit substrate on the first integrated circuit substrate;
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;
> a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical and mechanical connection bypasses the second integrated circuit substrate;
> a second electrical and mechanical connection between the second and third integrated circuit substrates; and
> a third electrical and mechanical connection between the first and second integrated circuit substrates. (Underline added.)

In support of the rejection of Claim 1, the Office Action states that Figure 5 of Morishita shows an electronic device comprising:

> ... a third integrated circuit electronic substrate 3 with connections/bumps 8 on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit electronic substrates;
>
> a first electrical and mechanical connection (from 1 to 3) between the first and third integrated circuit substrates wherein the first electrical and mechanical connection/bump to the second integrated circuit substrate....

Office Action, page 3. The Applicant respectfully submits, however, that Morishita fails to teach or suggest a first electrical and mechanical connection between first and third integrated circuit substrates with the first electrical and mechanical connection bypassing the second integrated circuit substrate (with the second integrated circuit substrate being between the first and third integrated circuit substrates).

As shown in Figure 5 of Morishita, all interconnections between the first chip 1 and the third chip 3 pass through the second chip 2 which is between the first and third chips 1 and 3. Interconnections between non-adjacent chips one and three (through chip 2) of Morishita are discussed in Morishita as follows:

> The third chip select pad 63b on the bottom surface of the first level semiconductor bear chip 1 is connected to the third chip select pad 63a on the top surface of the first level semiconductor bear chip 1. The third chip select pad 63a on the top surface of the first level semiconductor bear chip 1 is further connected through the connective bump 8 to the second chip select pad 62b on the bottom surface of the second level semiconductor bear chip 2. The second chip select pad 62b on the bottom surface of the second level semiconductor bear chip 2 is further connected to the second chip select pad 62a on the top surface of the second level semiconductor bear chip 2. The second chip select pad 62a on the top surface of the second level semiconductor bear chip 2 is further connected through the connective bump 8 to the first chip select thereof 61b on the bottom surface of the third level semiconductor bear chip 3. (Underline added.)

Morishita, col. 11, lines 47 to 62. Accordingly, Morishita fails to teach or suggest any electrical and mechanical connection between chips 1 and 3 of Figure 5 thereof that bypass chip 2.

For at least the reasons discussed above, the Applicant respectfully submits that Morishita fails to teach or suggest the recitations of Claim 1, and that Claim 1 is thus patentable. In addition, the dependent Claims 2-4, 6-8, 64-65, and 68 are patentable at least as per the patentability of Claim 1 from which they depend. The Applicant further submits that the

pending claims 2-4, 7-8, 64-65, and 68 are separately patentable because no prior art rejections have been applied to these claims.

CONCLUSION

Accordingly, the Applicant submits that all pending claims in the present application are in condition for allowance, and a Notice of Allowance is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues need to be addressed.

Respectfully submitted,

Scott C. Hatfield
Registration No. 38,176

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer Number 20792

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on May 2, 2007.

Signature: _____
Joyce Paoli